IN THE CLAIMS

Please cancel Claims 11 and 13 without prejudice or disclaimer.

Claim 1 (currently amended): 1. A driver circuit for driving a load with a differential signal, comprising:

a first output drive portion operably coupled to a power supply rail;

a second output drive portion coupled to the first output drive portion, a low voltage differential input signal, and further comprising output terminals coupled to the load, and operably coupled with

a ~~constant~~ current source, wherein the second output drive portion is operable to switch alternate polarity terminals of the load to the current source; and

a common mode compensation circuit coupled to the output terminals of the second output drive portion and the first output drive portion, wherein the common mode compensation circuit is operable to detect a common mode voltage associated with the load and generate a compensation signal in response thereto, wherein the first output drive portion is operable to vary an impedance associated therewith in response to the compensation signal, thereby regulating a common mode voltage associated with the load, whereby the differential signal is transmitted to the load at a high rate of speed with a high compliance of the common mode output even at high current loading conditions, while maintaining a ~~simple~~ pre-drive circuit with a wide common mode range,

wherein both when the load is a standard LVDS load, the load is driven by a standard LVDS compatible output, and when the load is a standard CML load, the load is driven by a standard CML compatible output.

Claim 2 (original): The system of claim 1, wherein the first output drive portion of the driver circuit comprises;

two bipolar transistors coupled in an emitter follower configuration, having a collector terminal of each bipolar transistor connected to the supply voltage, and a base terminal of each bipolar transistor connected together and to the compensation signal from the common mode compensation circuit, whereby the common mode compensation

circuit is operable to vary the impedance associated with each bipolar transistor of the first output drive portion based on the compensation signal in response to the common mode voltage from the load; and

two voltage dropping resistors associated with the two bipolar transistors, respectively, with a first terminal connected to an emitter of one of the bipolar transistors, and a second terminal coupled to the load and the second output drive portion of the driver circuit, respectively.

Claim 3 (original): The system of claim 1, wherein the power supply rail is a positive voltage.

Claim 4 (original): The system of claim 1, wherein the second output drive portion comprises:

two switching transistors individually adapted to receive one input of the low voltage differential input signal into a first terminal of one of the switching transistors, to couple a first terminal of the current source to a second terminal of each switching transistor, and wherein the first output drive portion and the load are coupled to a third terminal of the switching transistor, whereby the second output drive portion is operable to switch alternate polarity terminals of the load to the current source; and

the current source has a second terminal coupled with one of a power supply rail and ground, and is operable to set and supply a circuit current for the second output drive portion, whereby a differential signal, may be transmitted to the load at a high rate of speed.

Claim 5 (original): The system of claim 4, wherein one of the switching transistors comprises a MOS transistor.

Claim 6 (original): The system of claim 4, wherein one of the switching transistors comprises an NMOS transistor.

Claim 7 (original): The system of claim 1, wherein the common mode compensation circuit comprises:

a common mode voltage monitor circuit operable to provide the common mode voltage associated with a node of a voltage divider coupled across the output terminals for the load; and

a common mode error amplifier circuit operable to receive a reference voltage input and the common mode voltage from the common mode voltage monitor circuit, and generate a compensation signal to the first output drive portion in response thereto, whereby the impedance of the first output drive portion is adjusted such that voltage regulation of the common mode dc voltage is provided.

Claim 8 (original): The system of claim 7, wherein the voltage divider comprises two series connected resistors of about the same value.

Claim 9 (original): The system of claim 7, wherein the common mode error amplifier circuit comprises:

a reference voltage circuit operable to generate a reference voltage; and

an operational amplifier operable to receive the reference voltage at a non-inverting input and the common mode voltage at an inverting input of the operational amplifier, and further operable to generate the compensation signal to the first output drive portion, whereby the impedance of the first output drive portion is adjusted.

Claim 10 (original): The system of claim 9, wherein the reference voltage circuit generates a reference voltage of about 1.2 volts.

Claim 11 (canceled)

Claim 12 (currently amended): A driver circuit for driving a load with a differential signal, comprising:

a voltage mode output circuit operably coupled to a power supply rail;

a current mode switch circuit coupled to the voltage mode output circuit, a low voltage differential input signal, and further comprising output terminals coupled to the load, and operably coupled with a ~~constant~~ current source, wherein the current mode switch circuit is operable to switch alternate polarity terminals of the load to the ~~constant~~ current source; and

a common mode compensation circuit coupled to the output terminals of the current mode switch circuit and the voltage mode output circuit, wherein the common mode compensation circuit is operable to detect a common mode voltage associated with the load and generate a compensation signal in response thereto, and wherein the voltage mode output circuit is operable to vary an impedance associated therewith in response to the compensation signal, thereby regulating a common mode voltage associated with the load, whereby the differential signal is transmitted to the load at a high rate of speed with a high compliance of the common mode output even at high current loading conditions, while maintaining a ~~simple~~ pre-drive circuit with a wide common mode range,

wherein both when the load is a standard LVDS load, the load is driven by a standard LVDS compatible output, and when the load is a standard CML load, the load is driven by a standard CML compatible output.

Claim 13 (canceled)

Claim 14 (original): The system of claim 12, wherein the current mode switch circuit comprises two switching transistors which are operable to alternately conduct between an on-state current and an off-state current respectively, whereby the differential signal is transmitted to the load at a high rate of speed.

Claim 15 (original): The system of claim 14, wherein the on-state current is greater than the off-state current.

Claim 16 (original): The system of claim 14, wherein the off-state current is greater than zero.

Claim 17 (original): The system of claim 12, wherein the voltage mode output circuit of the driver circuit and the common mode compensation circuit comprises a low impedance voltage regulator circuit, whereby the common mode voltage associated with the load is regulated.

Claim 18 (currently amended): A method of driving a differential signal for high speed data transmission in transceiver, converter, and repeater devices comprising:

detecting a dc voltage associated with the differential signal across a load with a common mode voltage monitor circuit to provide a common mode voltage associated with a node of a voltage divider coupled across the terminals of the load;

applying the common mode voltage and a reference voltage to a common mode compensation circuit;

generating a compensation signal based on the common mode voltage and the reference voltage;

applying the compensation signal to a voltage mode output circuit;

adjusting the impedance of the voltage mode output circuit in response to the compensation signal, thereby regulating the common mode voltage associated with the load at a level set by the reference voltage;

inputting a low voltage differential input signal from a pre-drive circuit and the voltage regulated output from the voltage mode output circuit, into a second output drive portion;

<u>driving said load by both a standard LVDS compatible output when the load is a standard LVDS load and a standard CML compatible output when the load is standard CML compatible output,</u>

switching the transistors of the current mode switch circuit in response to the low voltage differential input signal, between low and high conduction levels established by the voltage mode output circuit impedance and a ~~constant~~ current source, thereby conducting a current which flows from the voltage mode output circuit, thru the load, and the current mode switch circuit, and a current which flows thru the voltage mode output circuit and the current mode switch circuit; and

transmitting a differential signal to the load at a high rate of speed, with a high compliance of the common mode output even at high current loading conditions, while maintaining a simple pre-drive circuit design with a wide common mode range.